IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

2812
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In re Patent Application of

Takahisa YAMAHA

Serial No.: 09/518,709

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Date: March 12, 2001

Group Art Unit: 2812

Examiner: --

For: MANUFACTURE METHOD FOR SEMICONDUCTOR WITH SMALL VARIATION IN MOS THRESHOLD VOLTAGE

Assistant Commissioner of Patents
Washington, D.C. 20231

SUBMISSION

Sir:

☒	Submitted herewith is a copy of art together with an art listing form listing the same for the convenience of the Examiner.
☒	The Japanese Publication(s) listed on the attached art listing form was/were cited in a Japanese Office Action issued in a related application. A copy of the Office Action is attached. English-language Abstracts have been provided for the references.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Assistant Commissioner of Patents, Washington, D.C. 20231, on March 12, 2001.

Steven I. Weisburd
Name of applicant, assignee or Registered Representative

Signature

March 12, 2001
Date of Signature

Respectfully submitted,

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SIW:sks/Enclosures